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(54) Exposure method.

(57) A method of manufacture of semiconductor devices, includes exposing different portions of a semiconductor substrate with a first exposure apparatus having a first exposure range ; placing and aligning the semiconductor substrate with respect to a second exposure range of a second exposure apparatus which range is larger than the first exposure range of the first exposure apparatus ; detecting an alignment error of each of the portions of the semiconductor substrate as covered by the second exposure range of the second exposure apparatus ; calculating an overall alignment error of those portions of the semiconductor substrate with respect to the whole second exposure range of the second exposure apparatus, on the basis of the detected alignment errors ; and controlling the exposure operation of the second exposure apparatus on the basis of the calculated overall alignment error.

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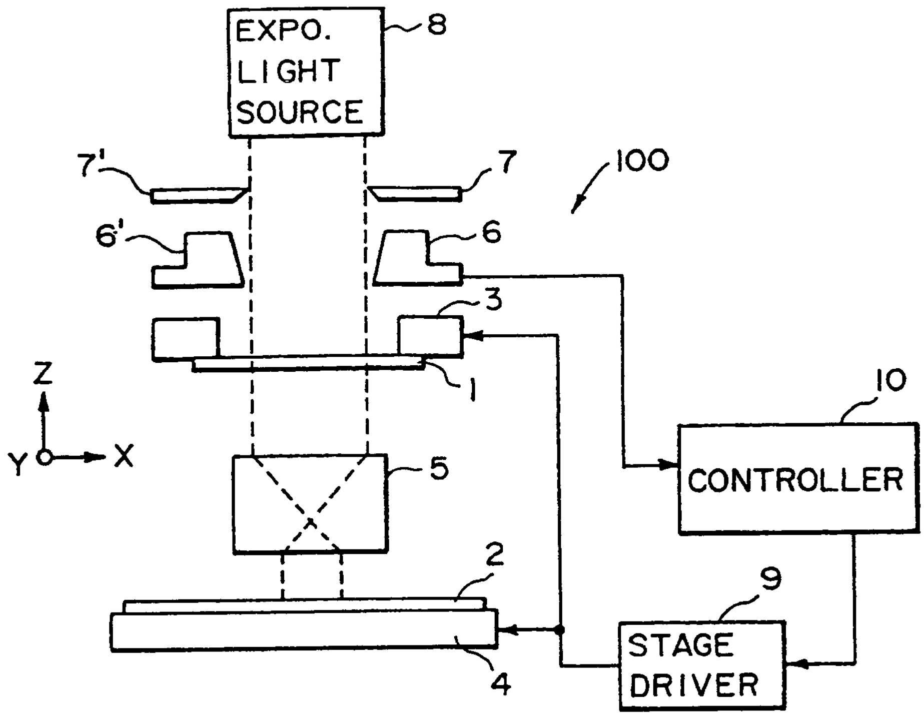
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7'
7
100
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1
Z
Y
X
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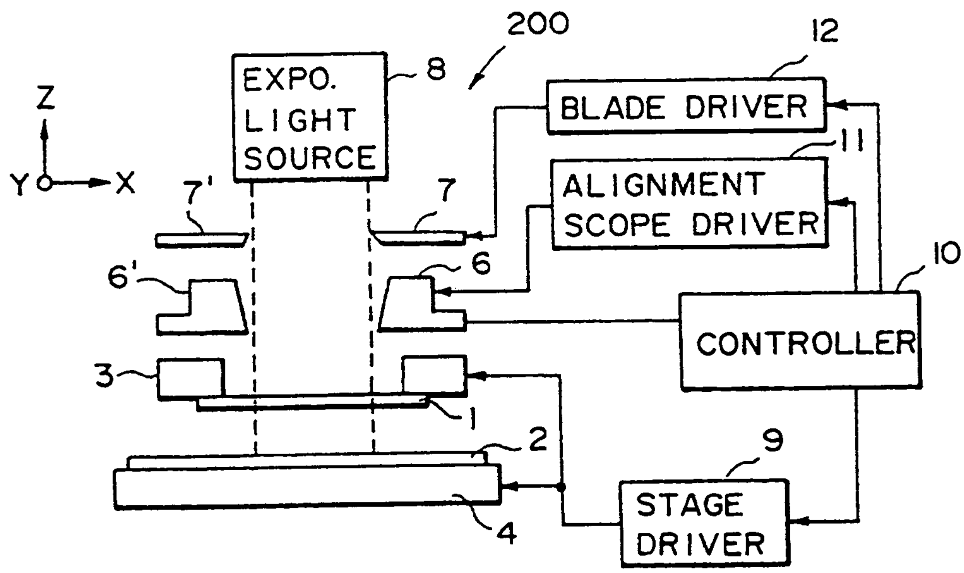
CONTROLLER
5
2
9
STAGE DRIVER
4

FIG. 1A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ALIGNMENT SCOPE DRIVER
7'
7
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CONTROLLER
3
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STAGE DRIVER
4

FIG. 1B

EXPOSURE METHOD

FIELD OF THE INVENTION AND RELATED ART

This invention relates to an exposure method suitably usable in production of fine patterns for manufacture of semiconductor devices. More particularly, the invention is concerned with an exposure method for sequentially exposing different portions (shot areas) of a semiconductor wafer to a mask to thereby print a pattern of the mask upon the shot areas of the wafer.

In a step-and-repeat type exposure apparatus, different shot areas of a semiconductor wafer are exposed sequentially to a mask (reticle), by which a circuit pattern formed on the mask is transferred to the shot areas of the wafer. As a radiation source for photolithographically exposing a wafer, some of this type exposure apparatuses use X-rays contained in synchrotron radiation, for example (hereinafter, this type exposure apparatus will be referred to as "X-ray stepper"), and some other ones use ultraviolet light such as, for example, g-line light or i-line light produced by a ultra-high voltage Hg lamp or, alternatively, laser light produced by a laser source such as an excimer laser (hereinafter, this type exposure apparatus will be referred to as "optical stepper").

As for the X-ray stepper, it is not easy to manufacture such a reduction projection lens system which is sufficiently practical to the use of X-rays. Although some X-ray steppers of reduction projection exposure type have been proposed, generally unit-magnification exposure is adopted wherein a mask and a wafer are placed opposed to each other with a small gap maintained therebetween. As is known in the art, the X-ray lithography is suited for the production of extraordinarily fine patterns.

As for the optical stepper, on the other hand, a reduction projection lens system having satisfactory performance to a particular light, to be used, can be manufactured relatively easily. Therefore, reduction projection exposure is widely used. In the reduction projection exposure, the width and precision of a pattern to be prepared on a mask or reticle can be wide as compared with those of a pattern which is to be actually printed on a wafer. Thus, there is an advantage of easiness in manufacture of the mask or reticle.

SUMMARY OF THE INVENTION

The manufacture of semiconductor integrated circuits or semiconductor devices include about ten to twenty exposure processes to one semiconductor wafer. Each exposure process is executed by an exposure apparatus having performance that satisfies required alignment precision and required linewidth precision for the pattern to be printed with that process. Also, for selection of such exposure apparatus, the productivity or cost of the apparatus should be considered.

It is a primary object of the present invention to provide an exposure method by which enhanced productivity or reduction in cost of an exposure apparatus is assured.

In accordance with an aspect of the present invention, there is provided a method of manufacture of semiconductor devices, comprising the steps of : exposing different portions of a semiconductor substrate with a first exposure apparatus having a first exposure range ; placing and aligning the semiconductor substrate with respect to a second exposure range of a second exposure apparatus which range is larger than the first exposure range of the first exposure apparatus ; detecting an alignment error of each of the portions of the semiconductor substrate as covered by the second exposure range of the second exposure apparatus ; calculating an overall alignment error of those portions of the semiconductor substrate with respect to the whole second exposure range of the second exposure apparatus, on the basis of the detected alignment errors ; and controlling the exposure operation of the second exposure apparatus on the basis of the calculated overall alignment error.

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B are schematic and diagrammatic views of a first exposure apparatus having a particular exposure range and a second exposure apparatus having a larger exposure range to which the present invention is applied, wherein Figure 1A shows an optical stepper, for example, and Figure 1B shows an X-ray stepper, for example.

Figure 2 is a flow chart showing sequential operations in an exposure method according to an embodiment of the present invention.

Figures 3A and 3B are schematic representations of wafer and mask patterns, in an occasion where in the Figure 2 embodiment the exposure range of the second exposure apparatus is restricted to a half.

Figures 4A and 4B are schematic representations of wafer and mask patterns, in an occasion where in the Figure 2 embodiment the exposure range of the second exposure apparatus is restricted to a quarter.

Figure 5 is a flow chart, for explaining the manner of detecting an overall alignment error with respect to the whole exposure range of the second exposure

apparatus.

Figure 6 is a flow chart, for explaining the manner of detecting an alignment error of each chip in the second exposure apparatus.

Figure 7 is a flow chart, generally illustrating the alignment operation.

Figures 8A and 8B are wafer and mask patterns which can be used in the second exposure apparatus of the Figure 2 embodiment.

Figure 9 is a flow chart, for explaining details of an exposure method according to another embodiment of the present invention.

Figures 10A and 10B are schematic representations of wafer and mask patterns, in an occasion where in the Figure 9 embodiment the exposure range of the second exposure apparatus is restricted to a half.

Figures 11A and 11B are schematic representations of wafer and mask patterns, in an occasion where in the Figure 9 embodiment the exposure range of the second exposure apparatus is restricted to a quarter.

Figure 12 is a flow chart, for explaining the manner of detecting an overall mask-to-wafer spacing adjustment error with respect to the whole exposure range of the second exposure apparatus.

Figure 13 is a flow chart, for explaining the manner of detecting a mask-to-wafer spacing adjustment error for each chip in the second exposure apparatus.

Figure 14 is a flow chart, generally illustrating the mask-to-wafer spacing adjustment.

Figures 15A and 15B are schematic representations of wafer and mask patterns which can be used in the second exposure apparatus, in the embodiment of Figure 9.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Generally, due to the limitation resulting from the projection range of a reduction projection lens, current optical steppers have a range to be exposed by a single shot (i.e. exposure range), of a size of about 15 - 20 mm square. On the other hand, X-ray steppers generally have a wider exposure range of about 30 mm square, at the maximum. It is now assumed that a first pattern of a first mask is printed on a layer of a semiconductor wafer by using a first exposure apparatus such as an optical stepper described above, having an exposure range (per one shot) of a size of 15 mm square and that, after predetermined treatment, a second pattern of a second mask is printed on the next layer of the wafer by using a second exposure apparatus such as an X-ray stepper described above, having an exposure range (per one shot) of a size of 30 mm square. Referring to Figures 8A and 8B, this example will be explained in detail. It is also assumed that the size of each semiconductor device to be formed on the wafer is 15 mm square which is equal to the size of the exposure range per one shot of the first exposure apparatus.

In the following description, reference character M denotes an alignment pattern formed on a mask, and reference character W denotes an alignment pattern formed on a wafer. The suffixes denote the order of disposition of semiconductor devices (hereinafter "semiconductor chips") formed on the wafer as well as that of the alignment patterns. For example, reference character W21 denotes a first alignment pattern of the second semiconductor chip of the wafer, and reference character M21 denotes an alignment pattern of the mask corresponding to the alignment pattern W21. In Figure 8A, each wafer pattern printed by the first exposure apparatus has a size of 15 mm square and, therefore, four semiconductor chips can be arrayed in the exposure range of the second exposure apparatus. Accordingly, within the exposure range of the second exposure apparatus, four sets of alignment patterns #1 (W11, W12), #2 (W21, W22), #3 (W31, W32) and #4 (W41, W42) are present.

Figure 8B shows alignment patterns of a mask to be used with the second exposure apparatus. Similarly, the mask to be used with the second exposure apparatus has four sets of alignment patterns #1 (M11, M12), #2 (M21, M22), #3 (M31, M32) and #4 (M41, M42). If only the second exposure apparatus, for example, is used so that all the exposure processes are executed with the same exposure range, it is sufficient that a mask to be used with the second exposure apparatus is equipped with one set of alignment patterns. However, if the first exposure apparatus is to be used additionally, the provision of four sets of alignment patterns is necessary. This will be readily understood, by taking into account a case where the first exposure apparatus is used after the second exposure apparatus is used.

Referring to the flow chart of Figure 7, the alignment process will be explained. As an example, the mask alignment patterns M31 and M22 and the wafer alignment patterns W31 and W22 are used. At step 1, by using the alignment patterns M31, M22, W31 and W22 and by using an alignment system (not shown), the mask-to-wafer alignment process is executed. At step 2, discrimination is made as to whether the remaining alignment error is less than a predetermined or not. If not, the sequence goes back to step 1, and the alignment process is repeated. If the alignment error is less than the predetermined, the alignment process is finished.

With the alignment process descried above, during the alignment error detection, all the alignment errors of the second pattern with respect to all the four first patterns (each providing a semiconductor chip) are not detected. For this reason, there is a possibility that the printed second pattern is largely deviated from any one of the four first patterns.

In one preferred form of the present invention, it is possible to ensure desired positional precision in pattern printing, with regard to all the zones (shot areas) of the wafer.

More specifically, in this aspect of the present invention, the semiconductor device manufacturing process is executed by using a first exposure apparatus and a second exposure apparatus having a wider exposure range, wherein, when the wafer is to be exposed through the second exposure apparatus, the alignment error measurement can be made selectively in regard to each zone having the same size as of the exposure range of the first exposure apparatus or in regard to each zone having a size equal to a multiple, by an integer, of the exposure range of the first exposure apparatus.

If the alignment error measured in respect to the exposure range of the second exposure apparatus, after repetitions of the alignment process, does not become smaller than a predetermined, the exposure range of the second exposure apparatus may be reduced stepwise.

Referring now to Figures 15A and 15B, description will be made of adjustment of the interval between a mask and a wafer (hereinafter "M/W interval") in an occasion where first and second exposure apparatuses having different exposure ranges are used.

Character M denotes an M/W interval adjustment pattern of a mask, while character W denotes an M/W interval adjustment pattern of a wafer. The suffixes denote the order of disposition of semiconductor chips formed on the wafer as well as that of the M/W interval adjustment patterns. For example, reference character W21 denotes a first M/W interval adjustment pattern of a second semiconductor chip on the wafer, and reference character M21 denotes an M/W interval adjustment pattern of the mask corresponding to the alignment pattern W21.

In this example, as shown in Figure 15A, each wafer pattern printed on the wafer by the first exposure apparatus has a size of 15 mm square and, therefore, four semiconductor chips are arrayed in the exposure range of the second exposure apparatus. Namely, within the exposure range of the second exposure apparatus, four sets of M/W interval adjustment patterns #1 (W11, W12, W13), #2 (W21, W22, W23), #3 (W31, W32, W33) and #4 (W41, W42, W43) are present on the wafer. Figure 15B shows M/W interval adjustment patterns of a mask to be used with the second exposure apparatus. Similarly, this mask is equipped with four sets of M/W interval adjustment patterns #1 (M11, M12, M13), #2 (M21, M22, M23), #3 (M31, M32, M33) and #4 (M41, M42, M43). If only the second exposure apparatus, for example, is used so that all the exposure processes are executed with the same exposure range, it is sufficient that the mask to be used with the second exposure apparatus is equipped with one set of M/W interval adjustment patterns. However, if the first exposure apparatus is to be used additionally, the provision of four sets of patterns is necessary. This will be readily understood, by taking into account a case where the first exposure apparatus is used after the second exposure apparatus is used.

Referring now to the flow chart of Figure 14, the mask-to-wafer interval adjustment process will be explained. As an, the M/W interval adjustment patterns M31, M22, M43 ; W31, W22 and W43 of the mask and the wafer are used. At step 101, by using the patterns M31, M22, M43 ; W31, W22 and W43 and by using an interval adjusting system (not shown), the mask-to-wafer interval is adjusted. At step 41, after the adjustment, discrimination is made as to whether the remaining error in the mask-to-wafer interval is less than a predetermined or not. If not, the sequence goes back to step 101, and the interval adjustment process is repeated. If the remaining error is less than the predetermined, the adjustment process is finished.

With the M/W interval adjustment process described above, during the interval error detection, all the mask-to-wafer interval errors of the second pattern with respect to all the four first patterns (each providing a semiconductor chip) are not detected. For this reason, there is a possibility that the second pattern is largely defocused on any one of the four first patterns.

In another preferred from of the present invention, it is possible to ensure desired M/W interval adjustment precision in pattern printing, to all the zones (shot areas) of the wafer.

More specifically, in this aspect of the present invention, the semiconductor device manufacturing process is executed by using a first exposure apparatus and a second exposure apparatus having a wider exposure range, wherein, when a wafer is to be exposed through the second exposure apparatus, the M/W interval adjustment error measurement can be made selectively in regard to each zone of the same size as of the exposure range of the first exposure apparatus or in regard to each zone which is equal to a multiple, by an integer, of the exposure range of the first exposure apparatus.

If the M/W interval adjustment error measured in regard to the exposure range of the second exposure apparatus, after repetitions of the M/W interval adjustment process, does not become less than a predetermined, the exposure range of the second exposure apparatus may be reduced stepwise.

In these aspects of the present invention, the semiconductor device manufacturing process can be executed by using a first exposure apparatus and a second exposure apparatus having a wider exposure range, while the alignment error and/or the M/W interval adjustment error of each semiconductor chip included in the exposure range of the second expos-

ure apparatus can be minimized.

Referring now to Figures 1A and 1B showing one preferred form of the present invention, Figure 1A illustrates a step-and-repeat type exposure apparatus 100 having an exposure range or zone (per one shot), upon a wafer 2, of a size of about 15 - 20 mm square, for example. Mask 2 is formed with a pattern prepared for manufacture of semiconductor devices, and this pattern is projected through the exposure range upon the wafer 2 by a reduction projection lens 5, in a predetermined reduced scale. The wafer 2 is held by a stage 4 which is movable stepwise by a predetermined distance in the X or Y direction each time the mask is illuminated with exposure light from an exposure light source 8 and, thus, the pattem of the mask 1 is printed on the wafer with the exposure light passing through the reduction projection lens 5. In this manner, the pattern of the mask 1 is printed on different shot areas on the wafer 2, sequentially. The exposure light source 8 of the exposure apparatus 100 supplies ultraviolet light such as g-line light, i-line light, excimer laser light or the like. The exposure light from the source 8 is directed to masking blades 7 - 7′ by which the range of illumination to the mask 1 is restricted. After this, the light impinges on the mask 1 which is held by a mask stage 3.

Alignment scopes 6 - 6′ are provided to detect the relative position of alignment patterns, provided on the mask 1 and the wafer 2, with respect to the X and Y directions, through the cooperations of the reduction projection lens 5. The result of detection is supplied to a controller 10. In response, the controller 10 calculates any positional error between the mask 1 and the wafer 2 with respect to the X and Y directions as well as any rotational error therebetween about the Z axis. Additionally, through a stage driver 9, the controller 10 controls the position of the mask stage 3 and/or the wafer stage 4 so as to correct these errors. Further, by using a measurement signal supplied from a measuring device (not shown), the controller 10 calculates the position of the wafer 2 in the Z direction as well as rotational errors (tilt) thereof about the X and Y axes. Similarly, through the stage driver 9, the controller controls the position of the mask stage 3 and/or the wafer stage 4 to adjust the wafer position.

After these adjustments, the exposure source 8 starts irradiation of exposure light and, after exposure through a predetermined period is effected, the exposure process is finished. After this, the stage 4 moves stepwise as described so as to place the next shot area of the wafer 2 in the exposure range, and similar operations are repeated.

Figure 1B illustrates a step-and-repeat type exposure apparatus 200 having an exposure range or zone (per one shot), upon the wafer 2, of a size of about 30 mm square, for example. Mask 1 is formed with a pattern prepared for manufacture of semiconductor devices, and this pattern is projected through the exposure range upon the wafer 2 at a unit magnification, wherein the wafer 2 is disposed opposed to and closed to the mask 1. The wafer 2 is held by a stage 4 which is movable stepwise by a predetermined distance in the X or Y direction each time the mask 1 is illuminated with exposure light from an exposure light source 8 and, thus, the pattern of the mask 1 is printed on the wafer 2 with the exposure light. In this manner, the pattern of the mask 1 is printed on different shot areas on the wafer 2, sequentially.

While the exposure light from the source 8 of the exposure apparatus 200 may be ultraviolet light such as g-line light, i-line light, excimer laser light or the like, preferably it comprises X-rays. The exposure light from the source 8 is directed to masking blades 7 - 7′ by which the range of illumination to the mask 1 is restricted. After this, the light impinges on the mask 1 held by a mask stage 3. The masking blades 7 - 7′ of the exposure apparatus 200 are movable along an X-Y plane, by means of a blade driver 12, such that the range through which the exposure light passes can be changed as desired.

Alignment scopes 6 - 6′ are provided to detect the relative position of alignment patterns of the mask 1 and the wafer 2, with respect to the X, Y and Z directions. The result of detection is supplied to a controller 10. In response, the controller 10 calculates any positional error between the mask 1 and the wafer 2 with respect to the X and Y directions, any error in the interval between them along the Z direction as well as rotational errors about the X, Y and Z axes. Through a stage driver 9, the controller 10 controls the position of the mask stage 3 and/or the wafer stage 4 so as to correct these errors. The alignment scopes 6 - 6′ of the exposure apparatus 200 are movable along the X-Y plane by means of an alignment scope driver 11, and therefore, any position within the exposure range can be observed through the alignment scope. Further, the controller 10 supplies drive instruction signals to the blade driver 12 and the alignment scope driver 11.

After the position and interval adjustment made under the influence of the controller 10, the exposure source 8 starts irradiation of exposure light. After the exposure through a predetermined period is effected, the exposure process is finished. Then, the stage 4 moves stepwise as described, so as to place the next shot area of the wafer 2 in the exposure range, and similar operations are repeated.

One preferred embodiment of the present invention will now be explained with reference to the flow chart of Figure 2. This embodiment pertains to an alignment process in an occasion where the exposure apparatus 100 having an exposure range of 15 mm square is used to execute pattern printing and then the exposure apparatus 200 having an exposure range of 30 mm square is used to execute super-

posed printing of a next pattern. It is assumed now that each semiconductor device has a size of 15 mm square and, therefore, the exposure range of the exposure apparatus 100 has the same size as of one semiconductor chip.

In the following description, reference character M denotes an alignment pattern of a mask 1, and reference character W denotes an alignment pattern of a wafer 2. The suffixes denote the order of disposition of semiconductor chips and alignment patterns. For example, reference character W21 denotes a first alignment pattern of a second semiconductor chip of the wafer 2, and reference character M21 denotes an alignment pattern of the mask 1 corresponding to that alignment pattern. The patterns already formed on the wafer 2 are those having been printed thereon by using the exposure apparatus 100.

In the exposure apparatus 200, at step 1, the alignment system comprising the alignment scopes 6 - 6', the controller 10, the stage driver 9 and the like, is used to execute the mask-to-wafer alignment with respect to the mask alignment patterns M31 and M22 (Figure 8B) and the wafer alignment patterns W31 and W22 (Figure 8A). Use of these marks is merely an example, and any other alignment patterns may be used. At step 2, for each of the zones (shot areas) #1 - #4 of the wafer, i.e., for each semiconductor chip, an alignment error E1, E2, E3 or E4 is detected and, from the detected alignment errors E1 - E4, an overall alignment error E throughout the current exposure range of the exposure apparatus 200 is determined. In this case, therefore, the alignment precision with regard to each semiconductor chip as well as the overall alignment precision throughout the exposure range of the second exposure apparatus can be detected. This will be explained later in greater detail, with reference to Figure 5.

At step 3, discrimination is made as to whether the detected alignment error E is less than a predetermined or not. If the result is affirmative, the alignment process is finished, and the exposure process of the wafer 2 with the exposure light from the source 8 starts. If the alignment error is not less than the predetermined, through step 4 the above-described operations are repeated by predetermined times. The number of repetitions is determined in accordance with required precision, throughput and the like. If desired alignment precision E is not obtainable even after the repetitions of alignment process, the sequence goes to step 5 whereat the masking blades 7 - 7' are actuated by the blade driver 11 so as to restrict the exposure range to a half. The wafer and mask patterns in an occasion where the exposure range is restricted to a half, are illustrated in Figures 3A and 3B.

At step 6, similarly to step 1, the alignment system is used to execute the mask-to-wafer alignment with respect to the mask alignment patterns M11 and M22 and the wafer alignment patterns W11 and W22. Use of these marks is merely an example, and any other alignment patterns may be used. At step 7, for each of the zones (shot areas) #1 and #2 of the wafer, i.e., for each semiconductor chip included within the current exposure range of the exposure apparatus 200, being restricted to a half, an alignment error E1 or E2 is detected and, from the detected alignment errors E1 and E2, the overall alignment error E throughout the half exposure range of the exposure apparatus 200 is determined.

At step 8, discrimination is made as to whether the alignment error E is less than a predetermined or not. If so, the alignment process is finished and the exposure process is executed with regard to the exposure range restricted to a half. If not so, the above-described operations are repeated by predetermined times. The number of repetitions is determined in accordance with required precision, throughput and the like. If desired alignment precision is not obtainable after the repetitions by predetermined times, at step 10 the exposure range is further restricted to a quarter of the original exposure range. The wafer and mask patterns as the exposure range is restricted to a quarter, are illustrated in Figures 4A and 4B.

At step 11, similarly to step 1, the alignment system is used to execute the mask-to-wafer alignment with respect to the mask alignment patterns M11 and M12 and the wafer alignment patterns W11 and W12. In this case, the exposure range of the exposure apparatus 200 has the same size as of that of the exposure apparatus 100, namely, that of each semiconductor chip. Accordingly, the inconveniences resulting from the difference in exposure range are removed.

At step 12, discrimination is made as to whether the aligment error is less than a predetermined. If so, the alignment process is finished and the exposure process starts. If not so, the above-described operations are repeated.

In the foregoing case, the exposure range is restricted to a half and then to a quarter, sequentially. However, the step of restriction to a half may be omitted, and the exposure range may be restricted directly to a quarter. This can be determined in accordance with required precision, throughput and the like.

Referring to Figure 5, details of the manner of determining an alignment error E throughout the exposure range of the second exposure apparatus, from alignment errors E1 - E4 of the zones #1 - #4 of the wafer, having been exposed with the exposure apparatus 100, will be explained.

At step 21, an alignment error of a semiconductor chip #1 is measured and, at step 22, the error E1 of the semiconductor chip #1 is calculated. Figure 6 is a flow chart showing details of such measurement and calculation.

At steps 31 and 32, with respect to an alignment

pattern W11 at a lower left part of the semiconductor chip #1 and an alignment pattern M11 of the mask 1 opposed to the alignment pattern W11, an X-axis (horizontal component) X11 and a Y-axis component Y11 of the alignment error between these alignment patterns are measured.

At steps 33 and 34, with regard to an alignment pattern W12 at an upper right part of the semiconductor chip #1 and an alignment pattern M12 of the mask 1 opposed thereto, an X-axis (horizontal) component X12 and a Y-axis component y12, in a direction perpendicular to the X axis, of the alignment error between these alignment patterns, are measured.

At step 35, the squares of these error components, respectively, are totaled, and the sum is used as the alignment error E1 of the semiconductor chip #1.

Referring back to Figure 5, at steps 23 - 28, alignment errors E2, E3 and E4 are detected with regard to the semiconductor chips #2, #3 and #4, in a similar manner as the semiconductor chip #1.

At step 29, the largest of the alignment errors E1 - E4 of four semiconductor chips is detected. The largest one is used as the overall alignment error E for the four semiconductor chips, namely, throughout the exposure range of the second exposure apparatus. To this alignment error E detected in such manner, the discrimination at step 3 in Figure 2 is executed as described hereinbefore. At step 8, the number of chips to which the alignment error E calculation is to be made, is reduced to two, from four.

Next, another preferred embodiment of the present invention will be explained with reference to the flow chart of Figure 9. This embodiment pertains to a process of adjusting the interval between a mask 1 and a wafer 2 in the Z direction, in an occasion where the exposure apparatus 100 having an exposure range of a size of 15 mm square is used to execute the pattern printing and, then, the second exposure apparatus 200 having an exposure range of a size of 30 mm square is used to superposedly print a next pattern on the wafer. Here, it is assumed that each semiconductor device has a size of 15 mm square. Thus, the size of the exposure orange of the exposure apparatus 100 is equal to that of each semiconductor chip.

Reference character M denotes an M/W interval adjustment pattern of the mask, and reference character W denotes an M/W interval adjustment pattern of the wafer. The suffixes denote the order of disposition of semiconductor chips and that of M/W interval adjustment patterns.

For example, reference character W21 denotes a first M/W interval adjustment pattern of a second semiconductor chip of the wafer 2, and reference character M21 denotes an M/W interval adjustment pattern of the mask corresponding to that adjustment pattern.

At step 101, an interval adjustment system comprising, for example, the alignment scopes 6 - 6', the stage driver 9, the controller 10 and the like, is used to execute the mask-to-wafer interval adjustment process, with respect to the M/W interval adjustment patterns M31, M22 and M43 of the mask and the M/W adjustment patterns W31, W22 and W43 of the wafer. Use of the patterns M31, M22, M43 ; W31, W22 and W43 is merely an example, and any other M/W interval adjustment patterns may be used.

At step 102, for each of the zones (shot areas) of the wafer, i.e., for each semiconductor chip, an M/W interval adjustment error E1, E2, E3 or E4 is detected and, from the detected errors E1 - E4, an overall M/W interval adjustment error E throughout the exposure range of the second exposure apparatus 200 is determined. In this case, therefore, the M/W interval adjustment error of each semiconductor chip as well as the overall M/W interval adjustment error throughout the exposure range of the exposure apparatus 200 can be detected. This will be described later in greater detail.

At step 103, discrimination is made as to whether the M/W interval adjustment error E is less than a predetermined. If so, the interval adjustment process is finished and the exposure process starts by use of the exposure light from the source 8. If not so, the above-described steps 101 - 103 are repeated by predetermined times (step 104). The number of repetitions is determined in accordance with required precision, throughput and the like. If desired interval adjustment precision is not obtainable as a result of repetitions of the predetermined number, at step 105, the masking blades 7 - 7' are displaced along the X-Y plane by the blade driver 12 so as to restrict the exposure range of the exposure apparatus 200 to a half.

The wafer and mask patterns as the exposure range is restricted to a half, are illustrated in Figures 10A and 10B.

At step 106, similarly to step 101, the interval adjustment system is used to execute the mask-to-wafer interval adjustment process, with respect to M/W interval adjustment patterns M11, M22 and M23 of the mask 1 and M/W interval adjustment patterns W11, W22 and W23 of the wafer 2. Use of the patterns M11, M22, M23 ; W11, W22 and W23 is merely an example, and any other M/W interval adjustment patterns may be used. At step 107, for each of the zones of the wafer included in the restricted exposure range, i.e., for each semiconductor chip, an M/W interval adjustment error E1 or E2 is detected and, from the detected errors E1 and E2, an overall M/W interval adjustment error E throughout the exposure range of the exposure apparatus 200, being restricted to a half, is determined.

At step 108, discrimination is made as to whether the obtained M/W interval adjustment error E is less than a predetermined. If so, the interval adjustment

process is finished and the exposure process starts. If not so, at step 109, the above-described operations are repeated by predetermined times. The number of repetitions is determined in accordance with required precision, throughput and the like. If desired M/W interval adjustment precision is not obtainable as a result of repetitions of the predetermined number, at step 110, the exposure range of the exposure apparatus 200 is restricted to a quarter of the original. The wafer and mask patterns as the exposure range is restricted to a quarter, are illustrated in Figures 11A and 11B.

At step 111, similarly to step 101, the interval adjustment system is used to execute the mask-to-wafer interval adjustment process with respect to the M/W interval adjustment patterns M11, M12 and M13 of the mask 1 and the M/W interval adjustment patterns W11, W12 and W13 of the wafer 2. In this case, the exposure range of the exposure apparatus 200 has the same size as of that of the exposure apparatus 100, namely, that of each semiconductor chip. Accordingly, the inconveniences resulting from the difference in size of the exposure range are removed.

At step 112, discrimination is made as to whether the detected M/W interval adjustment error is less than a predetermined. If so, the interval adjustment process is finished and the exposure process starts. If not so, the above-described operations are repeated.

While in the foregoing example, the exposure range of the exposure apparatus 200 is restricted to a half and then to a quarter, the step of restriction to a half may be omitted and the exposure range may be restricted directly to a quarter. This may be determined in accordance with required precision, throughput and the like.

Referring now to Figure 12, details of the manner of detecting the overall M/W interval adjustment error E throughout the exposure range of the exposure apparatus 200, from the M/W interval adjustment errors E1 - E4 of the four zones of the wafer, namely, the four semiconductor chips, will be explained.

At step 121, an M/W interval adjustment error of the semiconductor chip #1 is measured and at step 122, the error E1 of the semiconductor chip #1 is calculated.

Figure 13 is a flow chart, illustrating details of such measurement and calculation.

At step 131, by using an M/W interval adjustment pattern W11 at a lower left part of the semiconductor chip #1 and a corresponding adjustment pattern M11 of the mask 1, an M/W interval adjustment error d11 is measured.

At step 132, by using an M/W interval adjustment pattern W12 at an upper right part of the semiconductor chip #1 and a corresponding pattern M12 of the mask 1, an M/W interval adjustment error d12 is measured.

At step 133, by using an M/W interval adjustment pattern W13 at the lower right part of the semiconductor chip #1 and a corresponding pattern M13 of the mask 1, an M/W interval adjustment error d13 is measured.

At step 134, an average of these error components d11, d12 and d13 is calculated, and the obtained average is used as the M/W interval adjustment error E1 of the semiconductor chip #1.

Referring back to Figure 4, at steps 123 - 128, M/W interval adjustment errors E2, E3 and E4 are detected with regard to semiconductor chips #2, #3 and #4, in a similar manner as in the semiconductor chip #1.

At step 129, the largest of the M/W interval adjustment errors E1 - E4 of the four semiconductor chips is detected. The largest one is used as the overall M/W interval adjustment error E of the four semiconductor chips, namely, throughout the exposure range of the exposure apparatus 200. Then, discrimination is made at step 103. The remaining portion is essentially the same as that of the preceding embodiment.

As described hereinbefore, with the method of the present invention, even when exposure apparatuses having different exposure ranges are used in combination, the alignment errors and/or the M/W interval adjustment errors of all the semiconductor devices (chips) can be minimized. As a result, it is possible to ensure increased yield. Further, it is possible to provide semiconductor device manufacturing processes in which, by use of exposure apparatuses having different exposure ranges in combination, optimization is made in respect to the minimum linewidth, the productivity, the alignment precision and the like.

While the invention has been described with reference to the structures disclosed herein, it is not confined to the details set forth and this application is intended to cover such modifications or changes as may come within the purposes of the improvements or the scope of the following claims.

Claims

1. A method of manufacture of semiconductor devices, comprising the steps of :

   exposing different portions of a semiconductor substrate with a first exposure apparatus having a first exposure range ;

   placing and aligning the semiconductor substrate with respect to a second exposure range of a second exposure apparatus which range is larger than the first exposure range of the first exposure apparatus ;

   detecting an alignment error of each of the portions of the semiconductor substrate as covered by the second exposure range of the second

exposure apparatus ;

calculating an overall alignment error of those portions of the semiconductor substrate with respect to the whole second exposure range of the second exposure apparatus, on the basis of the detected alignment errors ; and

controlling the exposure operation of the second exposure apparatus on the basis of the calculated overall alignment error.

2. A method according to Claim 1, wherein, when the overall alignment error throughout the whole second exposure range is not less than a predetermined, the exposure range of the second exposure apparatus is narrowed.

3. A method according to Claim 1, wherein the first and second exposure apparatuses use the same type of light sources for exposure.

4. A method according to Claim 1, wherein the first and second exposure apparatuses use different types of light sources for exposure.

5. A method of manufacturing semiconductor devices, comprising the steps of :

exposing different shot areas of a semiconductor substrate by using a first exposure apparatus having a first exposure range ;

aligning the semiconductor substrate with respect to a mask set in a second exposure apparatus having a second exposure range larger than the first exposure range ;

measuring errors of those shot areas of the semiconductor substrate covered by the second exposure range of the second exposure apparatus, in respect to an interval to the mask ;

calculating an overall interval error throughout the whole second exposure range of the second exposure apparatus, on the basis of the errors measured at the measuring step ; and

controlling the operation of the second exposure apparatus on the basis of the calculated error.

6. A method according to Claim 5, wherein, when the overall interval error throughout the whole second exposure range is not less than a predetermined, the second exposure range of the second exposure apparatus is narrowed.

7. A method according to Claim 5, wherein the first and second exposure apparatuses use the same type of light sources for exposure.

8. A method according to Claim 5, wherein the first and second exposure apparatuses use different types of light sources for exposure.

9. A method of exposing a semiconductor substrate in which a first area is exposed, and subsequently a second area is exposed, the first and second areas overlapping but being of different sizes.

10. A method of exposing a semiconductor substrate comprising aligning it with respect to a first exposure apparatus and exposing it thereby, and aligning it with respect to a second exposure apparatus and exposing it thereby, the first and second exposure apparatuses having different exposure areas or different ranges of exposure areas.

11. A method of exposing a semiconductor substrate comprising aligning the substrate and another part and subsequently exposing an area of the substrate, in which the accuracy of the alignment of the substrate with the said other part is determined for a proposed exposure area, and if a predetermined alignment condition is not met for the proposed exposure area under predetermined circumstances, the proposed exposure area is reduced before the said exposure.

12. A method of exposing a semiconductor substrate comprising testing for a condition and subsequently exposing an area of the substrate, in which the size of the said area is selected in accordance with the result of testing for the said condition.

13. Apparatus for carrying out a method according to any one of the preceding claims.

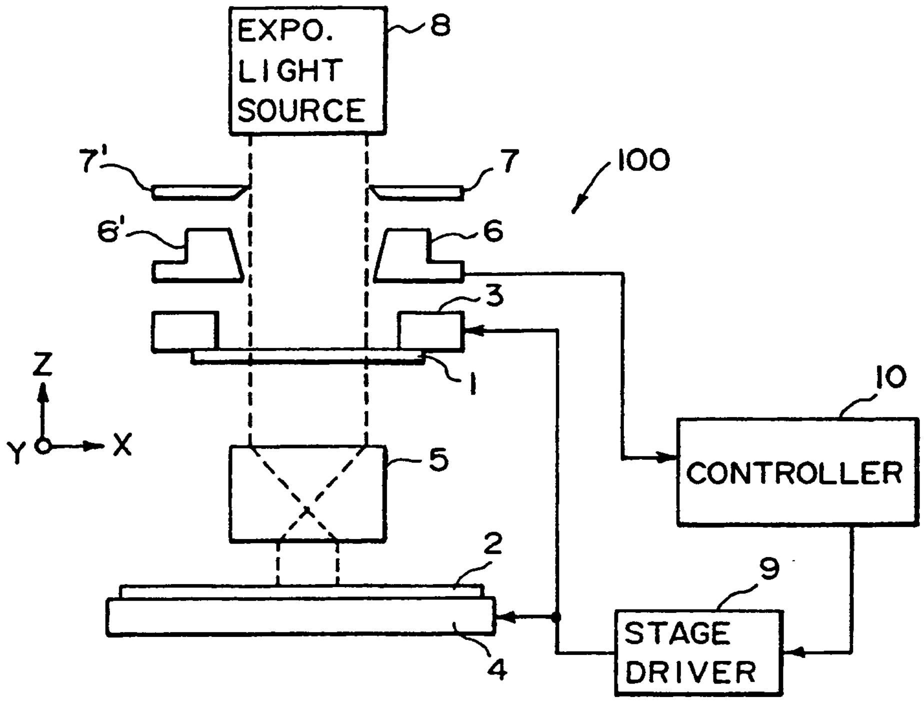

EXPO.
LIGHT
SOURCE
8
7'
7
100
6'
6
3
1
Z
Y
X
10
CONTROLLER
5
2
9
STAGE
DRIVER
4

FIG. 1A

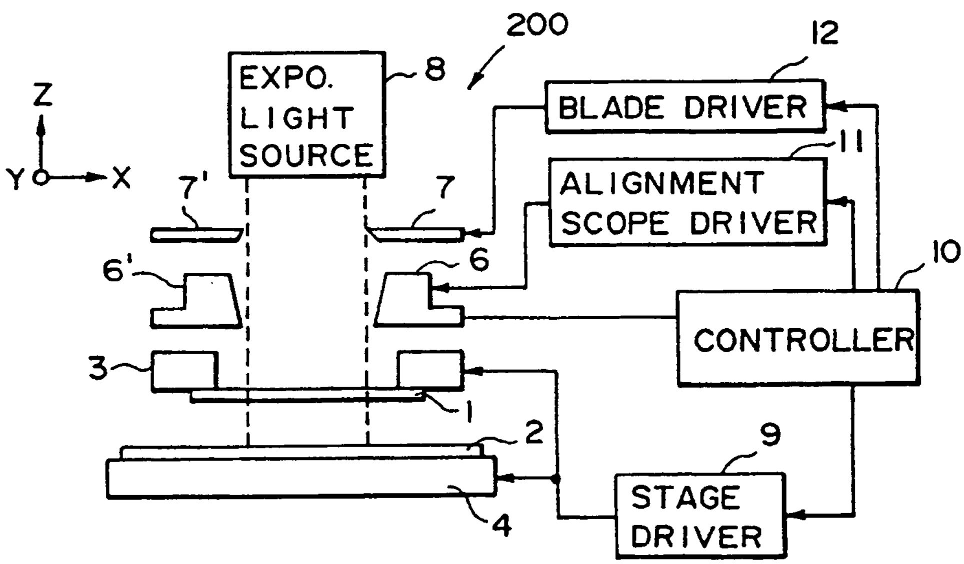
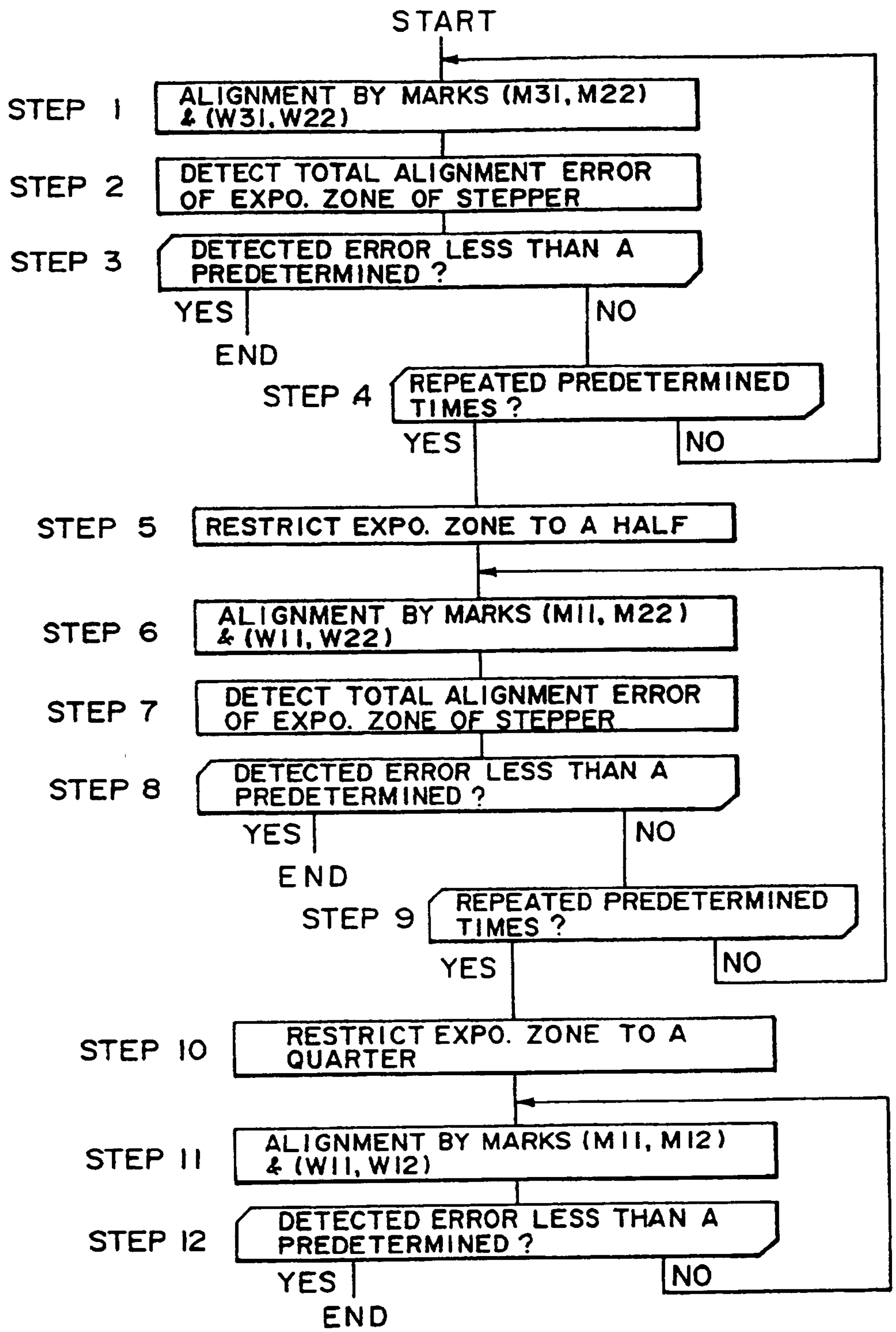

200
12
EXPO.
LIGHT
SOURCE
8
BLADE DRIVER
Z
Y
X
7'
7
11
ALIGNMENT
SCOPE DRIVER
6'
6
10
CONTROLLER
3
1
2
9
STAGE
DRIVER
4

FIG. 1B


START
STEP 1
ALIGNMENT BY MARKS (M31, M22) & (W31, W22)
STEP 2
DETECT TOTAL ALIGNMENT ERROR OF EXPO. ZONE OF STEPPER
STEP 3
DETECTED ERROR LESS THAN A PREDETERMINED ?
YES
END
NO
STEP 4
REPEATED PREDETERMINED TIMES ?
YES
NO
STEP 5
RESTRICT EXPO. ZONE TO A HALF
STEP 6
ALIGNMENT BY MARKS (M11, M22) & (W11, W22)
STEP 7
DETECT TOTAL ALIGNMENT ERROR OF EXPO. ZONE OF STEPPER
STEP 8
DETECTED ERROR LESS THAN A PREDETERMINED ?
YES
END
NO
STEP 9
REPEATED PREDETERMINED TIMES ?
YES
NO
STEP 10
RESTRICT EXPO. ZONE TO A QUARTER
STEP 11
ALIGNMENT BY MARKS (M11, M12) & (W11, W12)
STEP 12
DETECTED ERROR LESS THAN A PREDETERMINED ?
YES
END
NO

F I G. 2

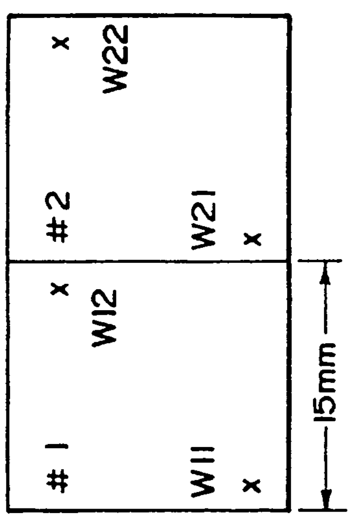


FIG. 3A
WAFER PATTERN

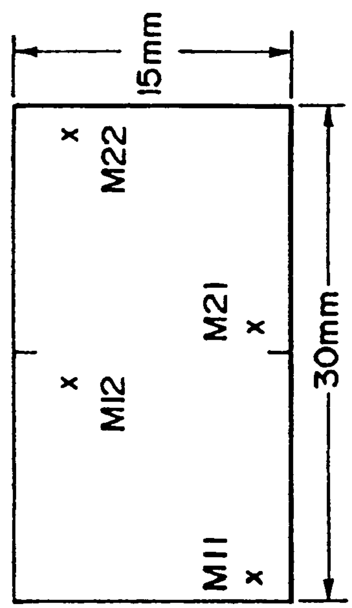


FIG. 3B
MASK PATTERN

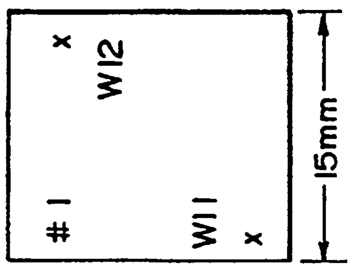


FIG. 4A
WAFER PATTERN

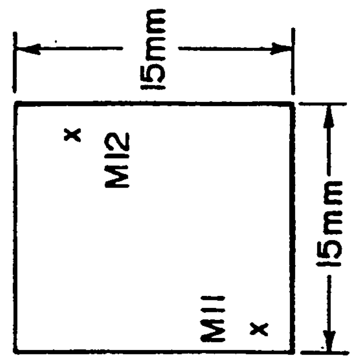


FIG. 4B
MASK PATTERN

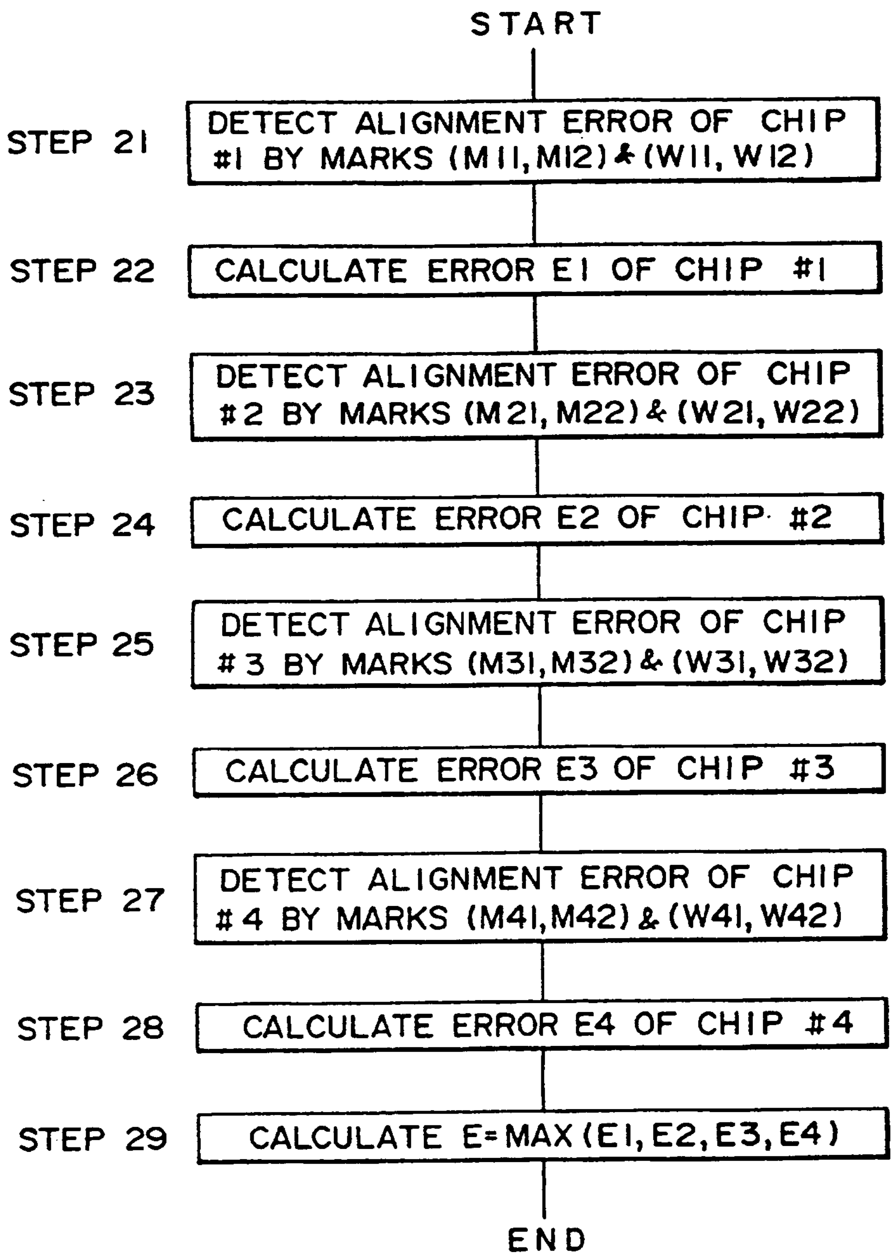

START
STEP 21
DETECT ALIGNMENT ERROR OF CHIP #1 BY MARKS (M11, M12) & (W11, W12)
STEP 22
CALCULATE ERROR E1 OF CHIP #1
STEP 23
DETECT ALIGNMENT ERROR OF CHIP #2 BY MARKS (M21, M22) & (W21, W22)
STEP 24
CALCULATE ERROR E2 OF CHIP #2
STEP 25
DETECT ALIGNMENT ERROR OF CHIP #3 BY MARKS (M31, M32) & (W31, W32)
STEP 26
CALCULATE ERROR E3 OF CHIP #3
STEP 27
DETECT ALIGNMENT ERROR OF CHIP #4 BY MARKS (M41, M42) & (W41, W42)
STEP 28
CALCULATE ERROR E4 OF CHIP #4
STEP 29
CALCULATE E=MAX (E1, E2, E3, E4)
END

FIG. 5

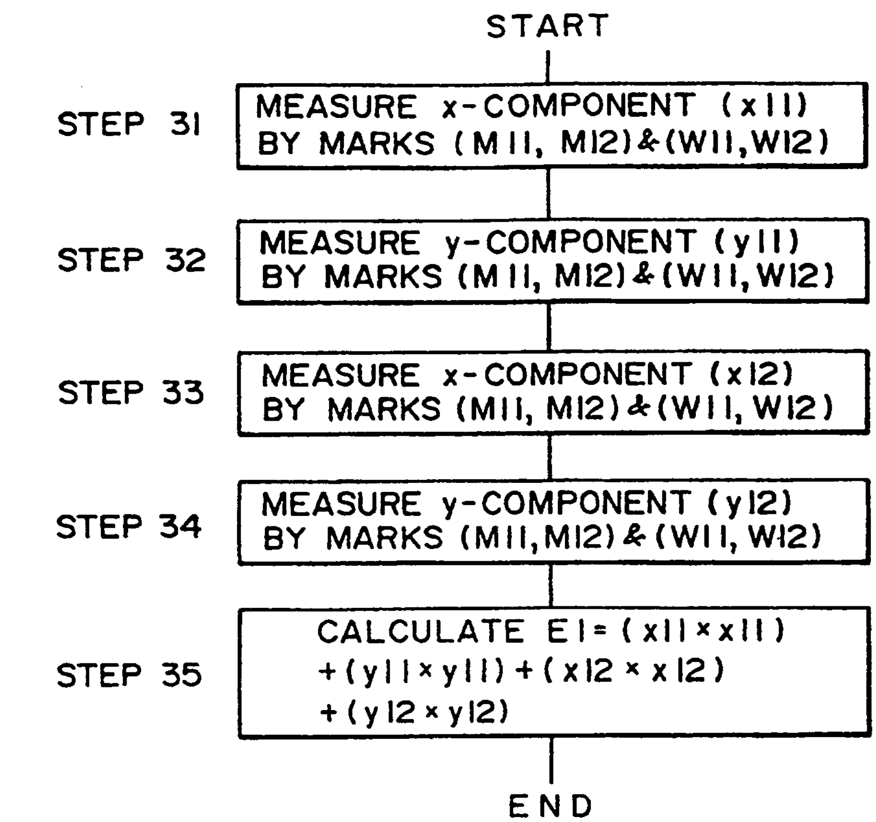

START
STEP 31
MEASURE x-COMPONENT (x11) BY MARKS (M11, M12) & (W11, W12)
STEP 32
MEASURE y-COMPONENT (y11) BY MARKS (M11, M12) & (W11, W12)
STEP 33
MEASURE x-COMPONENT (x12) BY MARKS (M11, M12) & (W11, W12)
STEP 34
MEASURE y-COMPONENT (y12) BY MARKS (M11, M12) & (W11, W12)
STEP 35
CALCULATE E1 = (x11 × x11) + (y11 × y11) + (x12 × x12) + (y12 × y12)
END

FIG. 6

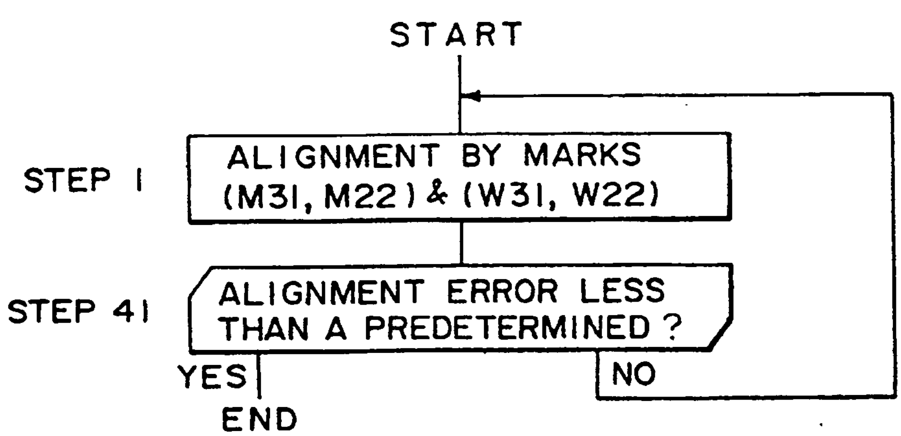
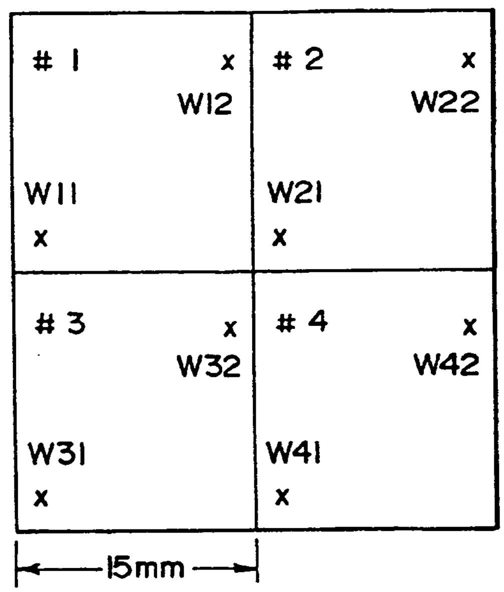
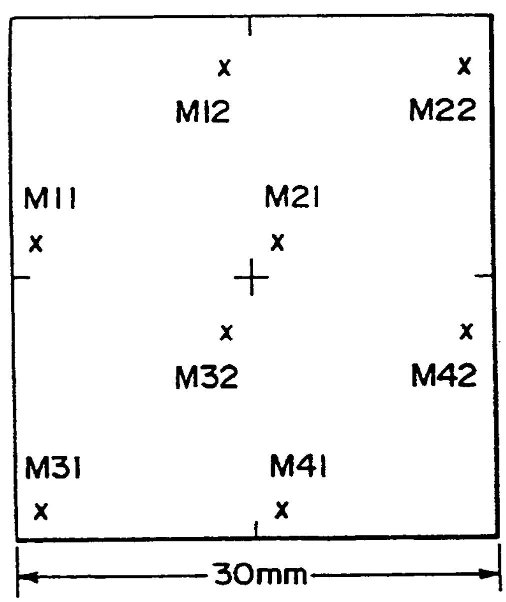

START
STEP 1
ALIGNMENT BY MARKS (M31, M22) & (W31, W22)
STEP 41
ALIGNMENT ERROR LESS THAN A PREDETERMINED ?
YES
NO
END

FIG. 7



F I G. 8A
WAFER PATTERN



F I G. 8B
MASK PATTERN

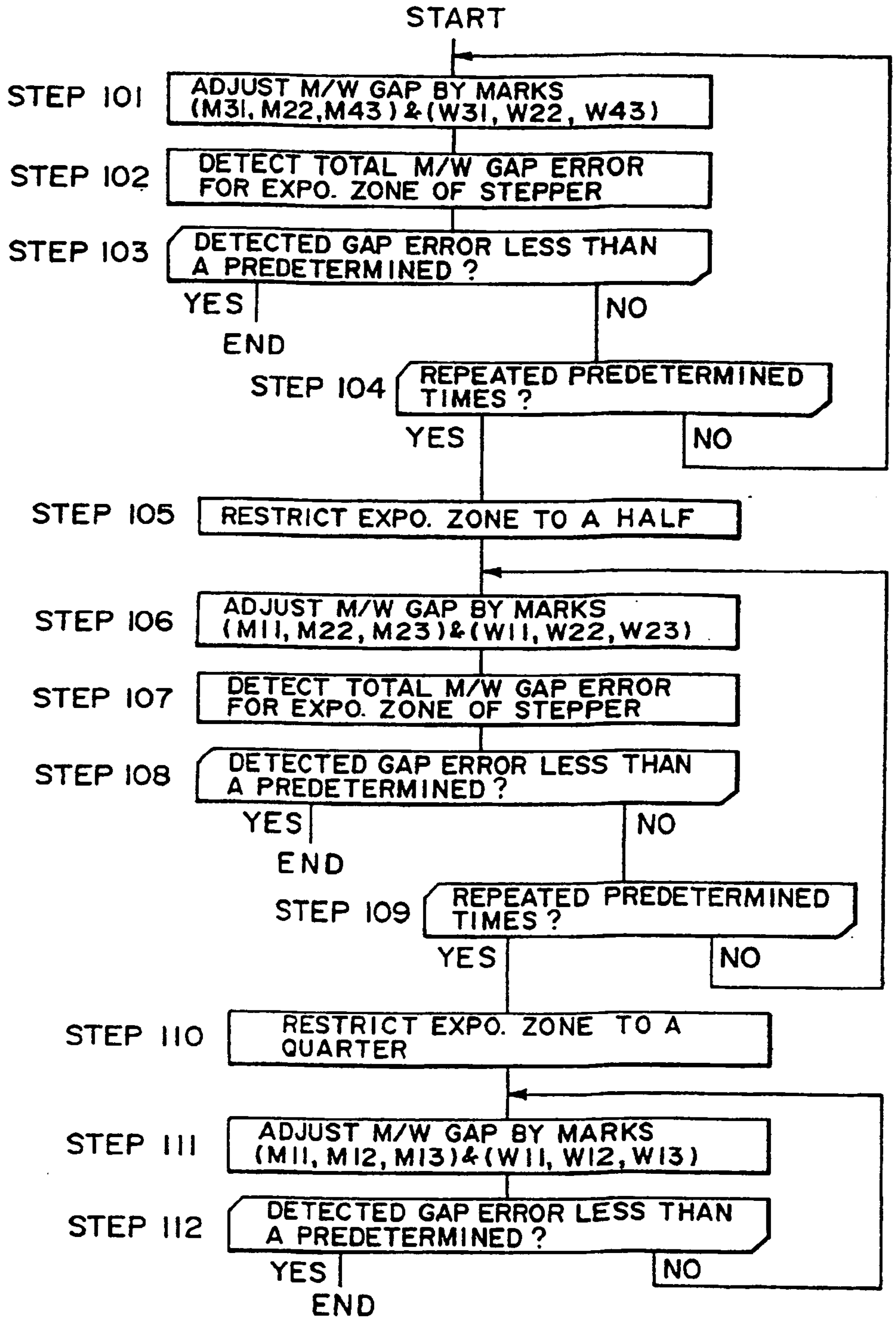

START
STEP 101
ADJUST M/W GAP BY MARKS (M31, M22, M43) & (W31, W22, W43)
STEP 102
DETECT TOTAL M/W GAP ERROR FOR EXPO. ZONE OF STEPPER
STEP 103
DETECTED GAP ERROR LESS THAN A PREDETERMINED ?
YES
END
NO
STEP 104
REPEATED PREDETERMINED TIMES ?
YES
NO
STEP 105
RESTRICT EXPO. ZONE TO A HALF
STEP 106
ADJUST M/W GAP BY MARKS (M11, M22, M23) & (W11, W22, W23)
STEP 107
DETECT TOTAL M/W GAP ERROR FOR EXPO. ZONE OF STEPPER
STEP 108
DETECTED GAP ERROR LESS THAN A PREDETERMINED ?
YES
END
NO
STEP 109
REPEATED PREDETERMINED TIMES ?
YES
NO
STEP 110
RESTRICT EXPO. ZONE TO A QUARTER
STEP 111
ADJUST M/W GAP BY MARKS (M11, M12, M13) & (W11, W12, W13)
STEP 112
DETECTED GAP ERROR LESS THAN A PREDETERMINED ?
YES
END
NO

FIG. 9

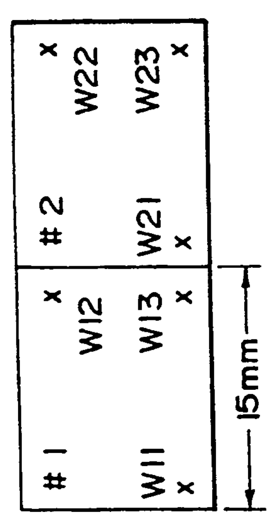


FIG. 10A
WAFER PATTERN

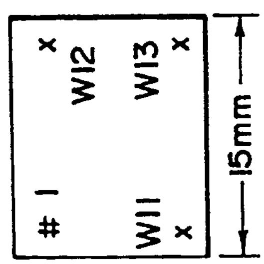


FIG. 11A
WAFER PATTERN

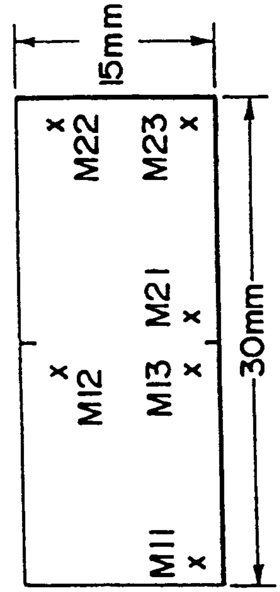


FIG. 10B
MASK PATTERN

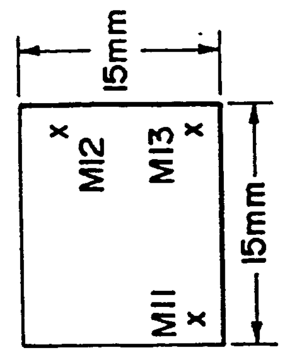


FIG. 11B
MASK PATTERN

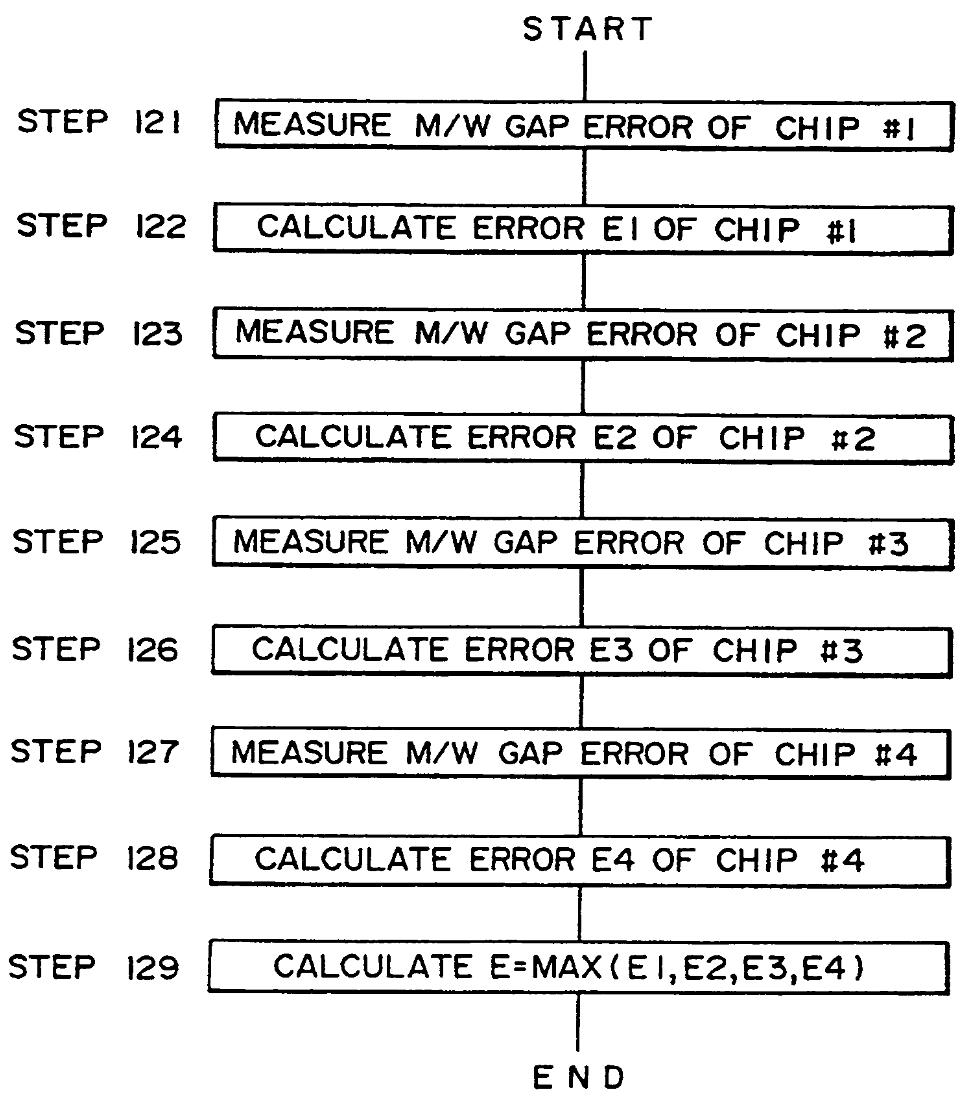

START
STEP 121
MEASURE M/W GAP ERROR OF CHIP #1
STEP 122
CALCULATE ERROR E1 OF CHIP #1
STEP 123
MEASURE M/W GAP ERROR OF CHIP #2
STEP 124
CALCULATE ERROR E2 OF CHIP #2
STEP 125
MEASURE M/W GAP ERROR OF CHIP #3
STEP 126
CALCULATE ERROR E3 OF CHIP #3
STEP 127
MEASURE M/W GAP ERROR OF CHIP #4
STEP 128
CALCULATE ERROR E4 OF CHIP #4
STEP 129
CALCULATE E=MAX(E1,E2,E3,E4)
END

FIG. 12

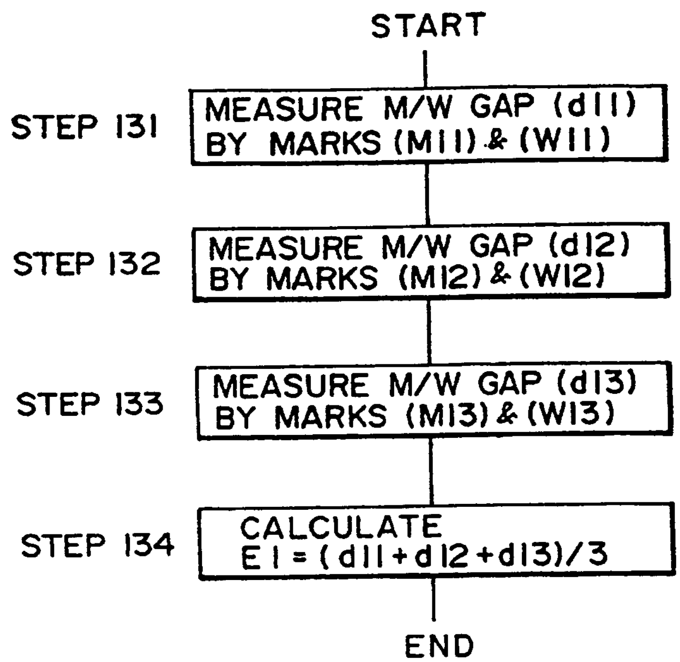

START
STEP 131
MEASURE M/W GAP (d11)
BY MARKS (M11) & (W11)
STEP 132
MEASURE M/W GAP (d12)
BY MARKS (M12) & (W12)
STEP 133
MEASURE M/W GAP (d13)
BY MARKS (M13) & (W13)
STEP 134
CALCULATE
E1 = (d11+d12+d13)/3
END

FIG. 13

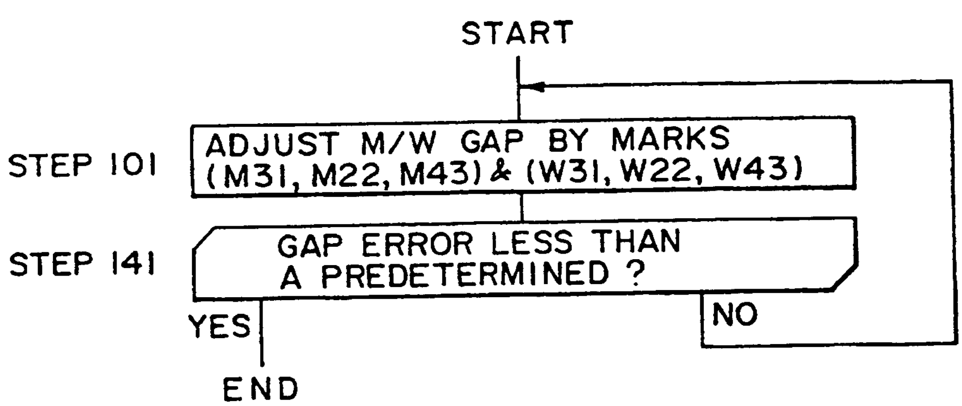

START
STEP 101
ADJUST M/W GAP BY MARKS
(M31, M22, M43) & (W31, W22, W43)
STEP 141
GAP ERROR LESS THAN
A PREDETERMINED ?
YES
NO
END

FIG. 14

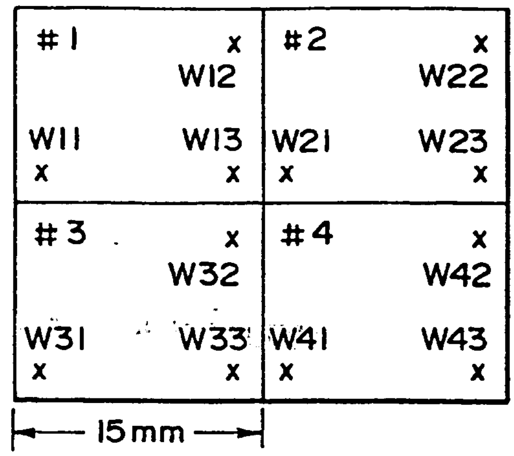


FIG. 15A
WAER PATTERN

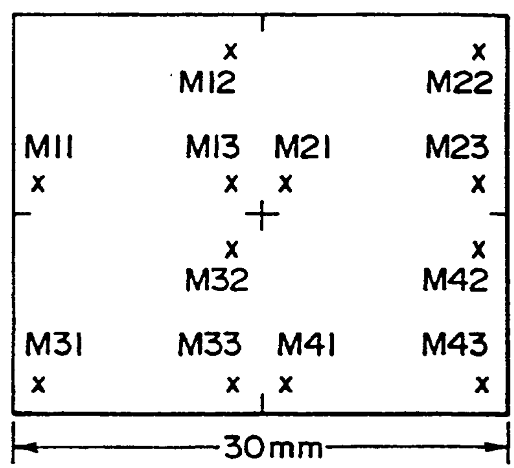


FIG. 15B
MASK PATTERN